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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,942	12/31/2001	Paras A. Shah	H052617.1140US0	2146

7590 11/10/2004

IP ADMINISTRATION, HEWLETT-PACKARD COMPANY
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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,942	SHAH ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-24* is/are allowed.

6)☒ Claim(s) *1-3,6-12 and 15-18* is/are rejected.

7)☒ Claim(s) *4,5,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 24 are presented for the examination.

2. Claims 5, 7, 8, 14, 16, and 17 are objected to because of the following informalities:

3. In the claims 5, and 14, define XOR as XOR [exclusive OR] at least once in the claim.

4. In the claims 7, 8, 16, 17, and 23, define PCI as PCI [peripheral component interface], and SCSI as SCSI [Small computer Systems Interface] at least once in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 – 3, 6 – 12,and 15 - 18 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Manning, US Patent 6,000,022.

7. As to claims 1, and 10, Manning discloses an apparatus and method of coupling signals between two operating circuits operating in different clock domains in computer system [300, fig. 10], comprising:

a. a first logic circuit [10, circuit A, fig. 4];

b. a second logic circuit [12, circuit B]; and

c. an interface [60, coupling circuit] coupling the first logic circuit [10] to the second logic circuit [12], wherein the interface includes:

(i) an input logic block [input logic block is inherent to coupling circuit 60] that receives an incoming data stream [Si] and a first clock [CLKA] from the first logic circuit [10], the input logic block provides [generates] an intermediate signal [S2], wherein if the incoming data stream includes a first asserted signal, the intermediate signal [intermediate signal] inverts its logic state [inverter inverts the logic state] [fig. 4 – 5]; and

(ii) an output logic block [output logic block is inherent to coupling circuit 60] coupled to [connected to] the input logic block [fig. 5], the output logic block receives the intermediate signal and a second clock [CLKB], wherein the output logic block provides to the second logic circuit an output signal [S3], the output signal [S3] is a second asserted signal for one clock period of the second clock [CLKB], when the output logic block detects a logic state change in the intermediate signal [col. 4, lines 35 – 49, col. 5, lines 10 – 65, fig. 4 – 5].

8. As to claims 2, and 11, Manning teaches that the first clock does not equal the second clock [two different clock domains] [col. 4, lines 52 – 53, col. 6, lines 50 – 52].

9. As to claims 3, and 12, Manning teaches an interface [coupling circuit, 60] which, includes a plurality of registers [42, read register, 52, write register] used in memory device [20'] therefore, he teaches to use these registers for metastability too [col. 8, lines 19 – 33, fig. 9].

10. As to claims 6, and 15, Manning discloses the first circuit an Intel IA-64 microprocessor [302, processor, fig. 10].

11. As to claims 7, and 16, Mannining discloses the second logic circuit is plurality of PCI devices [col. 8, lines 41 – 59].

12. As to claims 8, and 17, Manning discloses a bus bridge and an expansion bus [ISA, PCI] therefore he teaches a SCSI controller device too [col. 8, lines 41 – 59, fig. 10].

Allowable Subject Matter

13. Claims 4, 5, 13, and 14 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 19 – 24 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 7:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
November 2, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600 2100